# DVB-T2 Modulator

## bc006

The Binary Core DVB-T2 modulator bc006 – compliant with ETSI TR 302 755 V1.3.1 standard – is already available for different FPGA supports. The core is area-efficient and modular, thus making tailoring to your specific requirements straightforward. MFN mode with a single Transport Stream input can be used in the stand-alone version. SFN multi-PLP mode with T2-MI input is supported if Binary Core bc006 core is used along with an external DVB-T2 gateway (also available from Binary Core on request). Upgraded for T2-lite transmission.

# Features

- Bandwidth agility 1.7 MHz, 5 MHz, 6 MHz, 7 MHz, 8 MHz, or 10 MHz.
- Multi-PLP support with T2-MI stream generated by external DVB-T2 Gateway.
- Single Frequency Network (SFN) transmission mode (relative, absolute) supported with T2-MI stream generated by external DVB-T2 Gateway.
- T2-lite support (T2-base + T2-lite configuration are managed by a single modulator core).
- FFT sizes: 1K, 2K, 4K, 8K, 8K extended, 16K, 16K extended, 32K, 32K extended.
- Guard-interval fractions: 1/128, 1/32, 1/16, 19/256, 1/8, 19/128, 1/4.
- Scattered-pilot patterns: 8 different versions (PP1... PP8) matched to guard intervals.
- Continual pilots with improved optimization to reduce overhead, with respect to DVB-T.
- Supported code rates: 1/2, 1/3, 2/5, 3/5, 2/3, 3/4, 4/5 and 5/6 with normal and short FECFRAME. Additional supported code rates for T2-lite: 1/3, 2/5 with short FECFRAME.
- Data and L1-post signalling scrambling.

- L1-ACE offset correction and P2 bias balancing cells insertion.
- Supported modulation format: QPSK, 16-QAM, 64-QAM and 256-QAM.
- Rotated constellations, which provide a form of modulation diversity, to assist in the reception of higher code-rate signals in adverse channel condition.
- Extended interleaving, including bit, cell, time and frequency interleavers.
- Frame structure with special (short) identification symbol, for rapid channel scanning, signal acquisition, and frame-structure parameters transmission.
- Multiple Input Single Output (MISO) using the Alamouti technique.
- T2-MI interface support (Baseband data frames, L1 signalling frames, P2 bias balancing frames, DVB-T2 timestamp frames, FEF frames).
- Selective digital filter for shoulder attenuation.
- Matching to DAC clock frequency, thanks to a Numerically Controlled Re-sampler (NCR).
- Configurable pre-IFFT linear pre-filtering.

Optional features include

- Externally configurable non linear pre-distortion.
- Adaptive non linear pre-distortion using a post RF amplifier feedback signal.
- TS extraction from IP with SMPTE 2022-1/2.

A Demo version of the DVB-T2 modulator is available on request.

# DVB-T2 modulator block diagram

Current DVB-T2 modulator implementation supports a single input in Transport Stream format (mode A) in which the input TS (audio/video contribution) is modulated using the externally provided parameters (figure 1). Only mono-PLP MFN modulation is supported in this case. Mode adaptation and stream adpatation include: TS Rate Adaptation with PCR restamping, Normal/High Efficiency Mode processing, Null Packet Deletion, ISSY insertion and CRC-8 Encoding.

TS input stream may encapsulate a T2-MI stream (mode B) that contains multi-PLP data frames, signalling frames and timing information frames for SFN. Using different PID, TS input stream may encapsulate a T2-MI stream for T2-base component and a T2-MI stream for T2-lite component. Externally provided timing information includes a 10 MHz clock signal and a PPS signal for relative SFN (an additional second counter is needed to define an absolute time of emission). External memory is needed to manage MFN/SFN frame management.

IP to TS conversion with SMPTE 2022-1/2 FEC correction is also available.

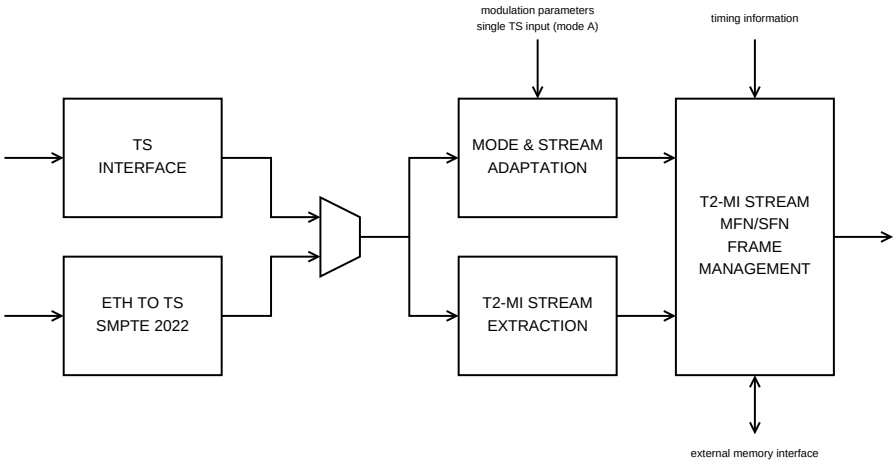


Figure 1: DVB-T2 modulator block diagram (I)

T2-MI Frame Management blocks are followed by coding, modulation and interleaving stages (figure 2). Different paths are provided for signalling and data. Data frames processing includes: data scrambling, BCH outer coding, LDPC inner coding, parity and column twist bit interleaving, mapping onto constellation, constellation rotation and cyclic delay, cell interleaving, time interleaver. External memory is needed to implement time interleaving. Signalling frames processing includes: L1-post signalling scrambling, BCH outer coding, LDPC inner coding, LDPC parity bits puncturing, bit interleaving, mapping onto constellation, L1-ACE correction.

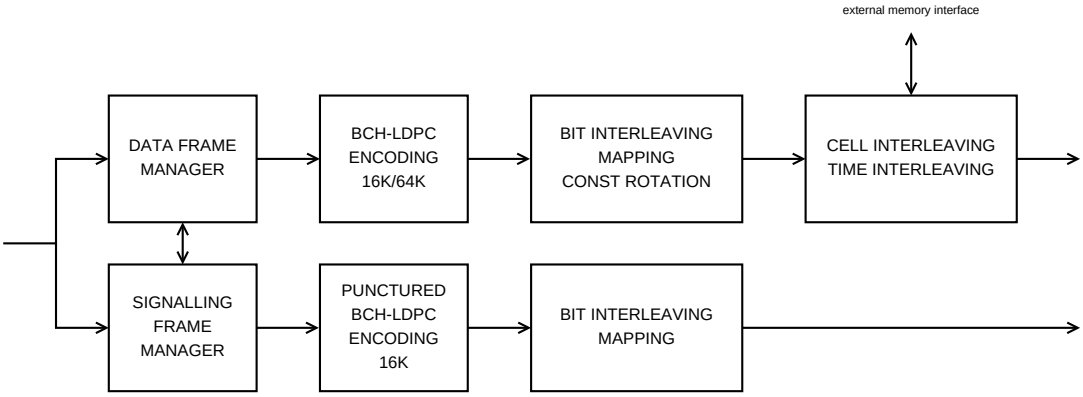


Figure 2: DVB-T2 modulator block diagram (II)

Eventually data and signalling are combined into the T2 frame structure (figure 3). Main tasks of this section are: DVB-T2 frame building (including FEF parts and T-base/T2-lite time division management), data PLPs and signalling management according to OFDM symbol type, insertion of bias balancing cells, frequency interleaver, MISO processing, pilot carrier insertion, configurable pre-IFFT linear filtering, OFDM symbol generation through IFFT Transform, guard interval insertion, preamble symbol insertion (P1 symbol), high selective filtering, numerically controlled re-sampler to match DAC clock frequency.

Non linear pre-distortion blocks (externally configurable or adaptive with feedback signal) are available on request.

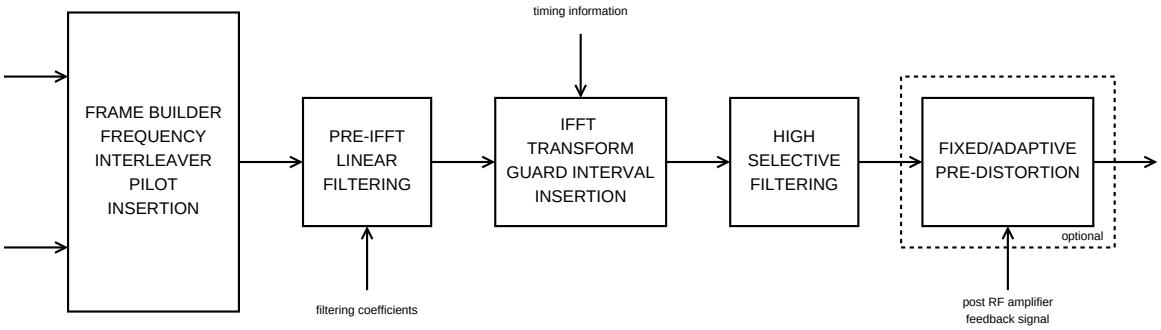


Figure 3: DVB-T2 modulator block diagram (III)

# DVB-T2 modulator configuration

The bc006 core in stand-alone version supports Multiple Frequency Network (MFN) transmission with a single Transport Stream (TS) input (see Figure 4).


Figure 4: DVB-T2 modulator in stand-alone version

Together with a DVB-T2 gateway (Binary Core bc007 or third party), Single Frequency Network (SFN) and multi-PLP transmission with a T2-MI stream input are supported (see Figure 5).

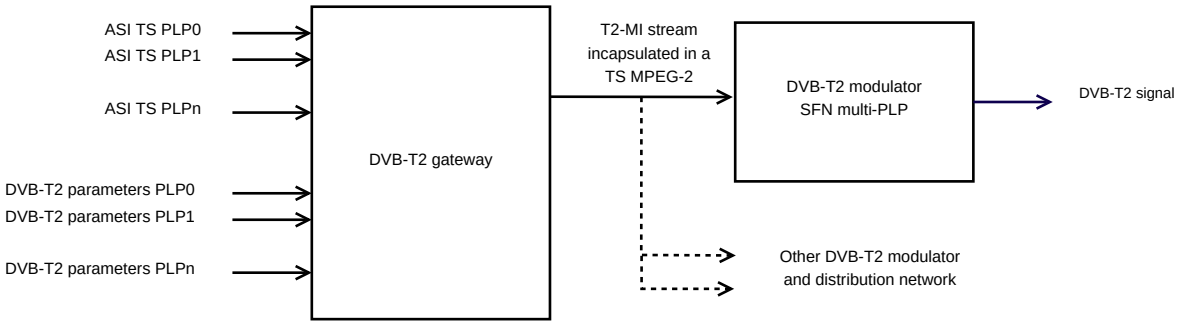


Figure 5: DVB-T2 modulator in multi-PLP version