DAB/T-DMB Modulator

bc012

Binary Core bc012 is an extremely compact DAB/T-DMB modulator, for implementation on low-cost FPGAs. Fully compatible with ETSI EN 300 401 standard, with register interface towards external or internal micro-processor for configuration and monitoring.

Features

- Supported standards: DAB, DAB+, T-DMB.
- DAB Modes: I, II, III, IV.
- All protection levels supported.
- MFN and SFN network modes.
- Optional linear and non-linear adaptive pre-correction.
- Input data: ETI(NI) or ETI(NA), compliant with G.703/G.704 standard (ETSI EN 300 799), with automatic detection.
- Optional seamless switch between two ETI inputs.
- Baseband or low-frequency digital IF output.

Main Functionalities

A high level block diagram of the DAB modulator is represented in Figure 1.

The core receives as input an ETI(NI, G.703) or ETI(NA, G.704), with a corresponding clock CK ETI, and a data valid DV ETI at 2.048 kHz. A further system clock CK SYS that is used throughout the modulator (typically synchronous with the DAC clock) with a frequency in the range 100÷150 MHz (which is adequate for implementation on low-cost FPGAs) can be also given as input. For testing purposes, an internally generated

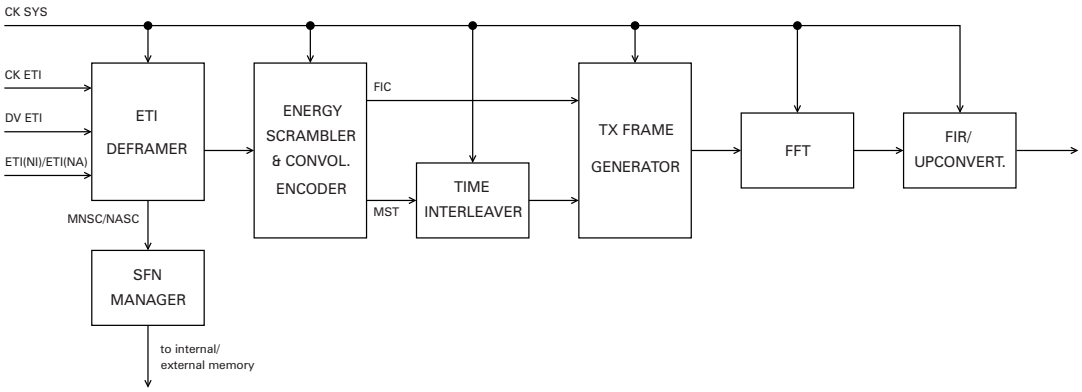

Figure 1: Block diagram of the DAB modulator

ETI stream is available.

The ETI DEFRAMER automatically detects NI or NA input, extracts FIC and MST data, relevant parameters from the ETI header, and MNSC or NASC service channels. The time stamps are extracted from these, for SFN functionalities. The buffering for SFN network mode of operation can be implemented either with an internal or an external memory.

Energy scrambling and convolutional coding is applied to both FIC and MST data, then MST is time-interleaved (no external memory required). After coding and interleaving, the transmission frame is constructed by first inserting a null symbol and a phase-reference symbol, followed by FIC and MST data. The time-domain signal is then generated by the FFT block. Finally the signal is filtered and upconverted to the desired output frequency (a fraction of the system clock).

The latency of the core has two main contributions. The latency of the actual modulator is the time difference between the start of an ETI frame with phase 0 at the input of the energy scrambler and the start of the corresponding null symbol at the output of the core. This delay depends on the system clock and on the Transmission Mode. Examples specified in Table 1 refer to a system clock of 150 MHz. The second contribution is due to the ETI deframer and is approximately equal to 25 ms for ETI(NA, G.704) and 0.14 ms for ETI(NI, G.703).

Transmission mode	**Modulator latency**
I	93.74 ms
II	23.57 ms
III	23.84 ms
IV	46.96 ms

Table 1: Example modulator latencies for a system clock frequency of 150 MHz